

## 1. INTRODUCTION

GLOBAL Positioning System (GPS) receivers for the consumer market require solutions that are compact, cheap, and low power. Manufacturers of cellular telephones, portable computers, watches, and other mobile devices are looking for ways to embed GPS into their products. Thus, there is a strong motivation to provide highly integrated solutions at the lowest possible power consumption. GPS radios consist of a front-end and a digital baseband section incorporating a digital processor. While for the baseband processor, cost-reduction reasons dictate the use of the most dense digital CMOS technology, for the front-end, the best option in terms of power consumption is a SiGe BiCMOS technology.

This explains why several commercial GPS radios consist of dual or multichip systems using the best technology option for the front-end and baseband processor. On the other hand, the implementation of a stand-alone GPS radio into a single chip in CMOS technology is appealing in terms of cost, and would speed up the integration of GPS capabilities into mobile products. This motivated the development of GPS macro blocks and radios in CMOS technology [1], [2].

However, the cost effectiveness of this solution depends on both reduction of external components and die area of the GPS radio. Since the silicon area of RF CMOS circuits, including on-chip inductors, does not shrink at the same rate as technology scaling, the reduction of the total cost poses a severe challenge.

This paper describes the design and measurement of a fully integrated CMOS GPS receiver targeting active antenna applications with an architecture geared to highest integration and minimal silicon area at the lowest possible power consumption (i.e., comparable to the best ones available [1], [2]).

The paper is organized as follows. The GPS system, architecture, and specifications are summarized in Section II, and the chip design is reported in Section III. Implementation details and experimental measurements are reported, respectively, in Sections IV and V. Finally, in Section VI, conclusions and comparison with the state of the art are given.

## 2. ARCHITECTURE AND SPECIFICATIONS

The GPS signal code is a direct-sequence spread spectrum, and the type of spread spectrum employed by GPS is known as binary phase-shift keying direct-sequence spread spectrum (BPSK DSSS). In a spread-spectrum system, data are modulated onto the carrier such that the transmitted signal has a larger bandwidth than the information rate of the data. The term “direct sequence” is used when the spreading of the spectrum is accomplished by phase modulation of the carrier.

The GPS satellites broadcast signals in a 20 MHz-wide band (L1 band) centered at 1.575 GHz. Two DSSS signals are broadcast in this band. They are known as the P code (or precision code) and the C/A code (or coarse acquisition code) (Fig.1).

For the GPS C/A code channel, most of the signal energy is located in a 2-MHz band which lies at the middle of the 20-MHz GPS-P code channel. At the antenna of a GPS receiver, the received signal power is typically 130 dBm. In the 2-MHz main lobe of the C/A code, the noise power (KTB) is 111 dBm with an associate signal-to-noise ratio (SNR) at the antenna of 19 dB.

In the past, several architectures have been used to relax the constraints of the GPS receiver using off-chip filtering and external components. For instance, a dual-conversion architecture with a first IF between 100–200 MHz and a second close to dc relaxes the constraints between selectivity and sensitivity of the receiver, i.e., allows using an external filter in front of the GPS low noise amplifier (LNA) with a lower quality factor. However, this comes with a penalty in terms of power consumption (two downconversions

and IF section running at high frequency) or in terms of bill of materials, since external IF filtering would be required. Another possibility is to use a single IF at a lower frequency with high quality factor off-chip RF filtering in front of the receiver. Clearly, the use of external components allows reducing the burden of the on-chip GPS receiver, and so its power consumption. Since we target a high level of integration, low-IF or zero-IF architecture with integrated IF filters must be selected. However, the presence of most of the energy at the center of the spectrum makes the use of a zero-IF architecture for a CMOS implementation difficult, due to the presence of flicker noise. For this reason, a low-IF architecture with image rejection has been selected in order to relax constraints on the external RF filter and to reduce the noise figure (NF) of the receiver. The associate penalty is an increased complexity and power consumption. An IF below 10 MHz guarantees a low energy at the image frequency and the feasibility of an integrated IF filters at a relatively low power consumption. Choosing an IF of 9.45 MHz, the required rejection is about 30 dB.

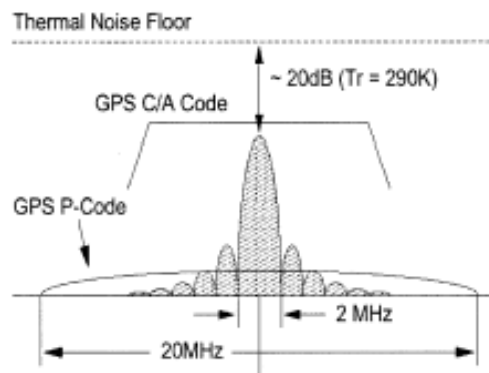


Fig. 1. GPS L1 band signal spectrum.

A detailed architecture block diagram of the receiver is shown in Fig. 2. The chip is fed with the GPS L1 signal from an active antenna, via an external

RF filter. This allows remote placement of the antenna from the receiver itself and relaxes noise requirements. A total voltage gain for the GPS receiver of 85 dB has been chosen. The combination of external LNA and GPS receiver brings the output signal (which is dominated by noise) to a level sufficiently high for the external analog-to-digital converter (ADC). For instance, if a 2-MHz band is considered, an external voltage gain between the antenna element and the chip input of 20 dB (including losses associated with the external filter and connectors) makes the total output noise power equal to  $-111\text{dBm} + 105\text{dB} \sim -6\text{dBm}$ .

In order to reduce power consumption and die area, the internal LNA uses a single-ended RF input. The LNA–mixer combination has an input 1-dB compression point ( $P1\text{ dB}$ ) of 28 dBm, therefore, the use of a low-quality external RF filter is enough to prevent blocking of the receiver (RX) chain from UMTS and GSM carriers.

The reported GPS radio downconverts the GPS L1 spread spectrum BPSK-modulated signal to an IF of 9.45 MHz (fully differential outputs) and provides two programmable CMOS

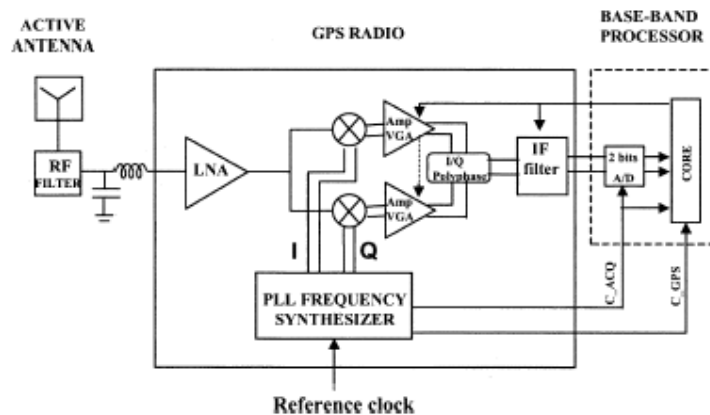


Fig.2. GPS Radio embedded in application from downconversion to code de-spreading.

TABLE I  
GPS RADIO SPECS

RF Frequency	1.575	GHz
Conversion Gain	85	dB
VGA range	60	dB
S11	< -10	dB
NF	5	dB
P1dB (Min Gain)	-28	dBm
Image Rejection IR	-30	dB
LO Frequency	1.565	GHz
Spurious Level	< -20	dBc
Phase Noise Integrated [500 Hz -1.5 MHz]	< 7°	rms
LO leakage to RF	< -60	dBm

Clock signals necessary for baseband ADC and synchronization of the correlator within the digital processor.

A summary of the GPS radio specs is reported in Table I.

### 3. CHIP DESIGN

As stated, the overall design has been geared to a high level of integration and reduction of silicon area at the lowest possible power consumption. Below, the detailed design choices in the various sections are described.

#### A. RF Section

The LNA has been designed to have a very low noise since it sets a lower bound for the total receiver sensitivity. A high voltage gain is necessary to sufficiently reduce the noise contribution of the following mixers.

A common source configuration with inductive degeneration provides high voltage gain and low NF, as shown in Fig. 3. In fact, in a narrow band, this structure allows achieving a noise factor close to the theoretical minimum. A single-ended LNA

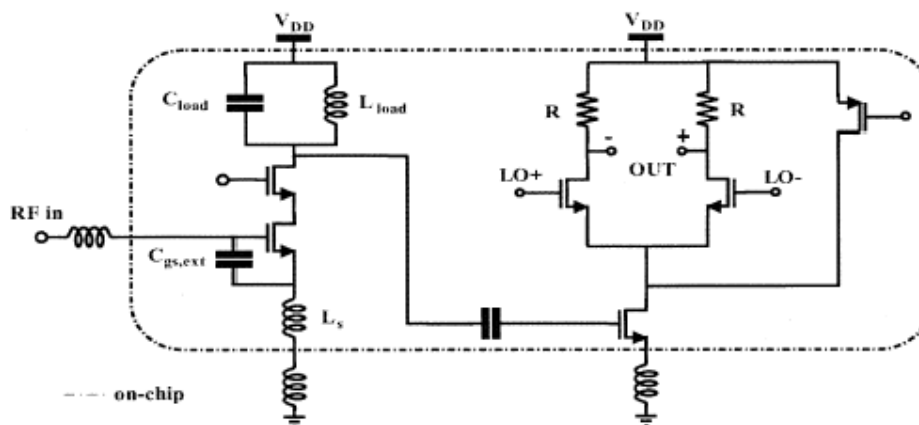


Fig. 3. LNA and mixer.

has been preferred to a balanced one to reduce power consumption and silicon area. The input of the mixer is still single ended, but from its output, the signal is taken in a differential fashion. In this topology, at a given frequency, there is an optimum device size for which the sum of gate induced and thermal noise has a minimum. Because of the strong sensitivity of the gate-induced current noise to the intrinsic gate capacitance (it follows a square law), an improvement can be obtained with the introduction of an additional capacitance  $C_{gset}$  placed in parallel to the intrinsic gate capacitance  $C_{gs}$  of the input transistor [3]. The insertion of this capacitance adds a degree of freedom to play with to achieve a better compromise between thermal and induced-gate noise. Therefore, a new optimum condition, with a lower noise figure minimum, can be achieved. This is paid by a slightly lower transconductance gain.

For the single-ended version, an input matching of 50 has been chosen because a higher value results in a worse external disturbances rejection. With a current consumption of 2 mA, the LNA features NF dB.

The LNA is followed by the - mixers that are ac-coupled to the LNA and are based on a modified Gilbert cell (Fig. 3). The mixers can be directly driven by the on-chip frequency synthesizer or by a single external local oscillator (LO) signal that drives an integrated RF polyphase filter. Improved linearity and reduced noise are achieved by subtracting dc current from the switching pair.

The load is a simple resistor. The current consumption is 1.5 mA for each mixer with an input P1 dB of 12 dBm.

## B. IF Section

After downconversion, the signal is amplified using a variable-gain amplifier (VGA) with 20-dB gain programmability (Fig. 2). A second-order integrated passive polyphase filter has been used to recombine the I and Q signal path [4]. The polyphase filter is an  $RC$  structure with inputs and outputs symmetrically disposed (Fig. 4). The relatively small ratio between the signal band and IF frequency allows building the combiner as the cascade of two  $RC$  passive poly-phase filters. A rejection of 30 dB across the 2-MHz band is achieved for  $\pm 20\%$   $RC$  time constant spread.

The IF filter is centered at 9.45 MHz. To fit the 2-MHz GPS band, even in presence of component values variations, the nominal transfer function features a larger bandwidth (6 MHz) than the one needed (2 MHz). However, a ripple in the GPS band (8.45–10.45 MHz) lower than 0.5 dB is guaranteed in any case. To optimize the power consumption for a given linearity and noise, an active  $RC$  solution has been chosen. The filter is built as a cascade of a bandpass and a low-pass cell, implementing a fourth-order transfer function (Fig.5). The filter also provides an antialiasing function before the baseband ADC (Fig. 2), assuring 20-dB attenuation at 28 MHz.

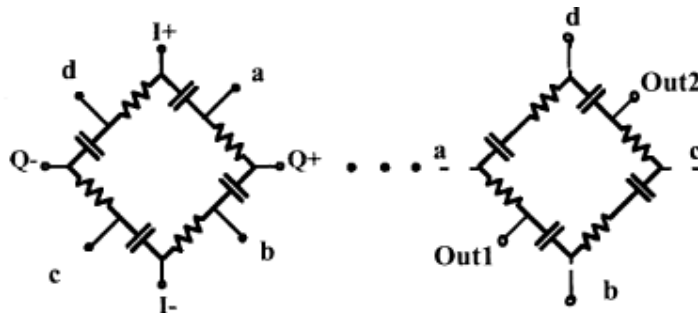


Fig. 4. Second-order IF polyphase.

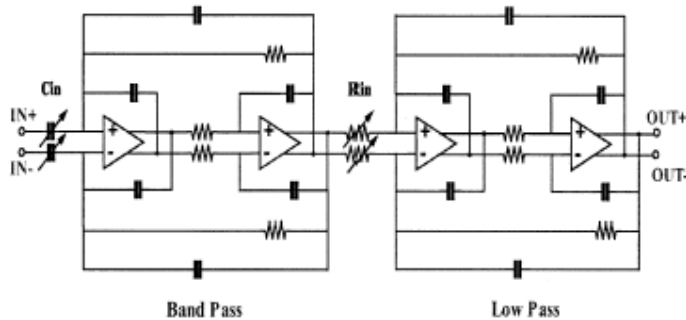


Fig. 5. IF filter.

A gain programmability of 40 dB (10–30 dB) in two stages has been implemented in the filter by digitally selecting the value of and. As the gain is programmed, constant input impedance should be maintained, so as not to affect the frequency response of the previous passive polyphase filter. This condition is achieved using the solution shown in Fig. 6. As far as the second biquad cell is concerned, a relatively high sensitivity of its pole position on the value of the cell gain has been observed. This is due to the different feedback conditions in

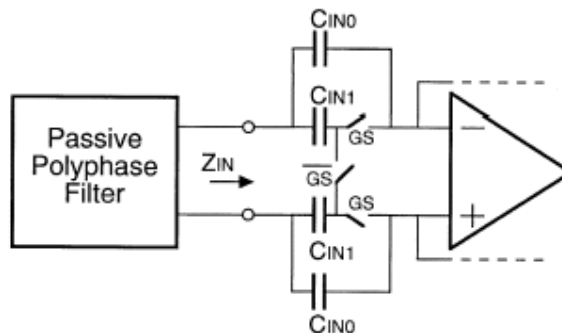


Fig.6. Interface between polyphase and first biquad.

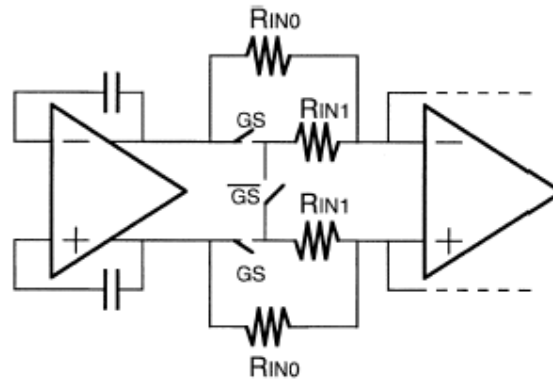


Fig.7. Connection between the first and the second biquad cells.

which the first opamp is operating. This problem has been overcome by using the scheme of Fig. 7. In this case, for any gain value, the total impedance for the feedback factor is always the same, and no pole deviation is then observed.

The opamp used in the filter and VGA uses a two-stage topology in order to keep sufficiently high gain even with a resistive load. Each differential opamp performs a dc gain of 54 dB with 7 pF//8 k load, which is the worst operation condition, and 200-MHz unity gain frequency. The filter exhibits a measured -4 dBm IIP3 (with a maximum gain level) and a simulated input referred noise of 15 nV/sqrtHz.

### C. Synthesizer

The synthesizer, depicted in Fig. 8, provides LO quadrature signals for the image-reject mixer and two clock signals needed to synchronize the correlator inside the external baseband processor. As for the previously described blocks, the main concern has been a high level of integration and reduction of silicon area at the lowest possible power consumption. The requirement of high integration and the need to reduce risks of LO pulling due

to off-chip components have driven the choice of a fully integrated voltage-controlled oscillator (VCO) and loop filter.

For this application, we took advantage of the low requirements on phase noise and spurious rejection using a ring oscillator within a wide-band phase-locked loop (PLL) instead of an inductance-capacitance ( $LC$ ) VCO. This choice resulted in a dramatic reduction of the silicon area, since it does not require integrated inductors or varactors. Furthermore, the ring oscillator directly provides  $I$ - $Q$  quadrature LO signals needed by the image-reject mixer and simplifies the portability of the GPS radio to a pure CMOS process with associated low-quality factor on-chip inductors. The use of a ring oscillator requires a wide-band PLL to reduce its contribution to the total phase noise. The added benefit of this choice is the integration of the loop filter in a limited silicon area. This is highly desirable to reduce the risk of VCO pulling due to external interferences coupled through the wire bondings. A 500-kHz band is implemented with 12 pF in parallel with the series of 300 pF and 6.4 k $\Omega$ .

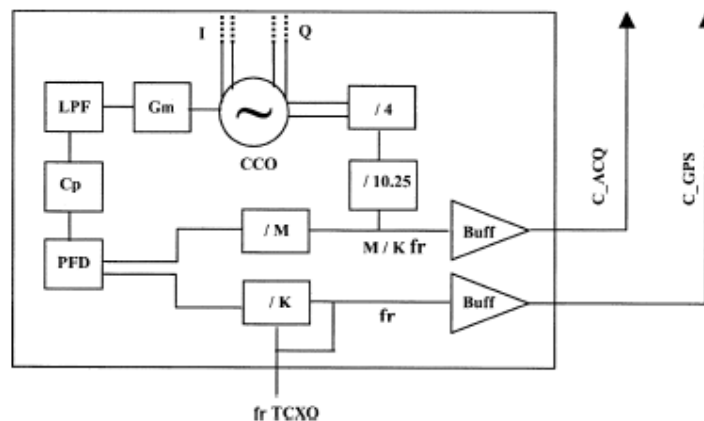


Fig. 8. PLL synthesizer.

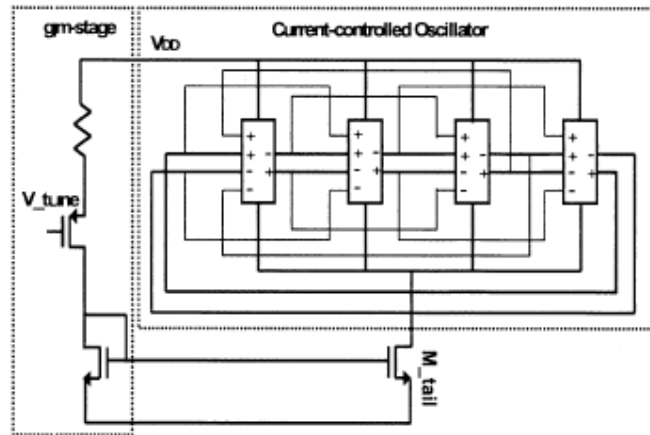


Fig. 9. VCO: dual paths indicated with thin lines.

The ring oscillator is implemented, cascading a transconductance stage to a current-controlled oscillator (CCO) (Fig. 9). The basic CCO cell, together with the tail current generator ( $M_{tail}$ ) is depicted in Fig. 10. Alternate delay paths, shown in Fig. 10 with thin lines, are used to achieve higher oscillation frequencies with the same power budget [5]. The dual scheme is implemented using the complementary pMOS inputs of each cell of the CCO, reported in Fig. 10. The cascade combination of the stage and the CCO yields a typical of 800 MHz/V. Such a high value allows compensating for all process spreads and temperature variations, and can be accepted due to the on-chip integration of the loop filter that reduces risks of LO pulling.

The total current consumption of the VCO is 2.8 mA.

A total dividing ratio of  $M*41$  has been introduced, where  $M$  is a programmable integer between 1 and 16. This allows the use of multiple TXCO references as clock reference with. The GPS radio has been characterized with and . In order to reduce overall power consumption and complexity, the 41 divider has been implemented with a divide-by-four prescaler, followed by a low-power fractional-10.25 divider.

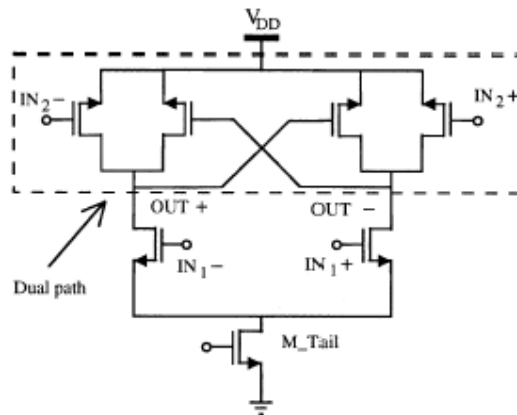


Fig. 10. Inverter used in the CCO. In dashed box: the pMOS inputs used by the dual paths.

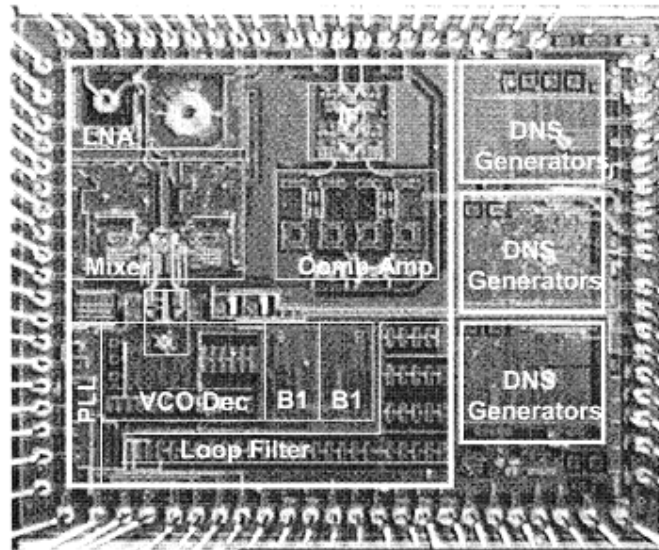


Fig. 11. GPS radio plus DNS generators.

The charge pump circuit is implemented to maximize the output voltage range due to the reduced supply voltage. Both the UP and DOWN portion of the circuit are realized as rail-to-rail switched pMOS and nMOS current mirrors and feature a speedup circuit to allow higher comparison frequencies. The saturation voltages of the output pMOS and nMOS transistors limit the maximum and minimum allowed loop-filter voltage to  $\sim 200\text{mV} \sim V_{\text{dd}}$ ,  $-200\text{mV}$ . The charge pump current injected into the loop filter is  $0.9\text{mA}$ .

#### 4. IMPLEMENTATION DETAILS

The GPS radio has been integrated in a 0.18-  $\mu\text{m}$  RF CMOS process with six metal levels, nMOS in excess of 55 GHz, high linearity 0.85-fF/ $\mu\text{m}$  MIM capacitances and 10-  $\text{cm}$  substrate resistivity. The availability of the triple well allows isolation of the nMOS transistors from the substrate. High quality factor MOS varactors are available, while for inductors is about 7 at 1.6 GHz.

A photograph of the fabricated test chip is shown in Fig. 11. This includes the GPS radio and three digital noise and spurs (DNS) generators test structures integrated on the same die to experimentally compare the immunity of the GPS radio to substrate noise with different substrate resistivity. Without bond pads, the GPS radio measures  $2 \times 1.8 \text{ mm}^2$ . The single-ended LNA ( $0.36 \text{ mm}^2$ ), placed at the top left corner, is isolated from the digital circuitry by placing the mixer at its bottom and folding around it the combiner-preamp and the IF filter. The VCO with its decoupling capacitances (VCO Dec in Fig. 11) and the integrated loop filter take, respectively,  $0.38 \text{ mm}^2$  and  $0.42 \text{ mm}^2$ . Two divide-by-four prescalers are placed on top of the VCO. One is used inside the PLL, the other offers a dummy load to the ring oscillator in order to keep precise  $I$ - $Q$  matching (normally turned off). The same divide-by-four prescaler can be used (turned on) to measure PLL phase noise. The two bias generators are labeled as B1 in Fig. 11.

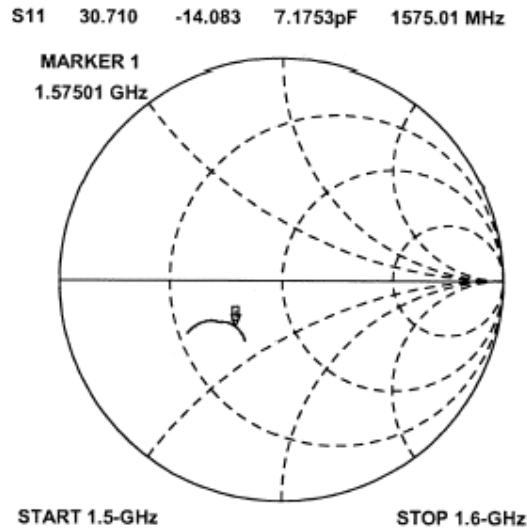


Fig.12. Measured S11.

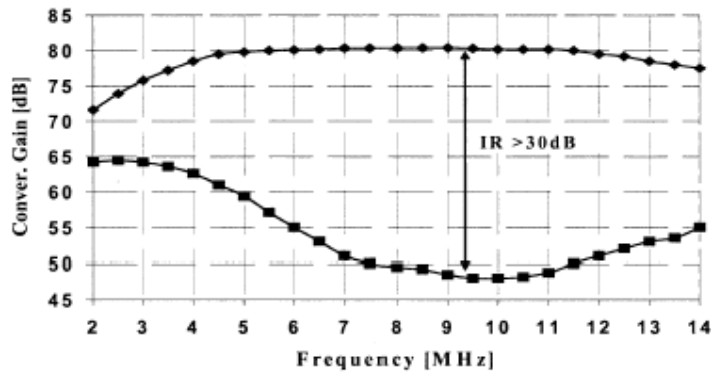


Fig.13. Image rejection bandwidth at IF.

The GPS radio has been housed in a standard 52-pin package (VFQFPN52) that allowed multiple ground downbondings to a common ground slug; each critical building block has a dedicated ground connected to its local p well. All dedicated grounds are connected by bond wires to the common ground slug. The return path of the LNA uses two separated (and orthogonal) ground pins. Patterned ground shields have been introduced under the inductor and the RF pads to reduce substrate losses. All pins are protected against electrostatic discharge (ESD).

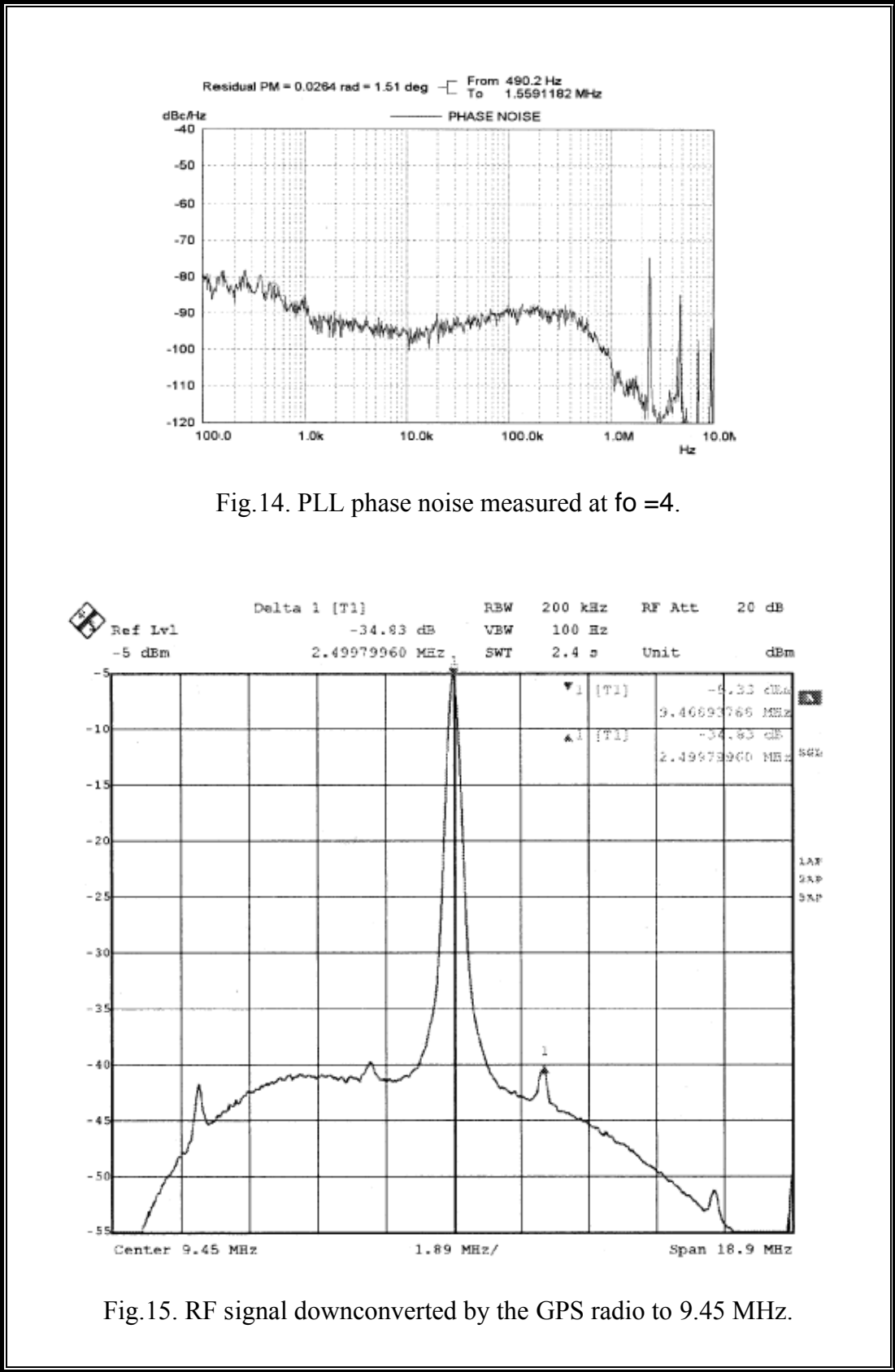


Fig.14. PLL phase noise measured at fo =4.

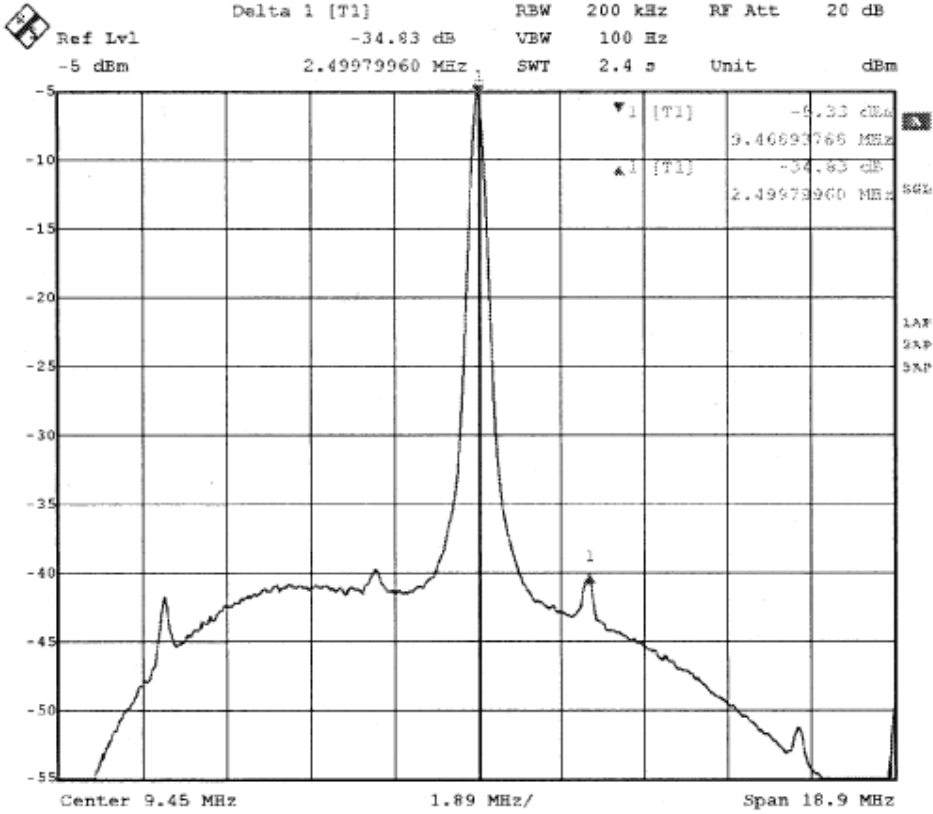


Fig.15. RF signal downconverted by the GPS radio to 9.45 MHz.

## **5. EXPERIMENTAL RESULTS**

The full GPS radio (i.e., receiver chain RX and synthesizer working together), housed in a VFQFPN52 package and soldered into an application board, has been characterized with the three DNS generators turned off. The RX features S11 dB, NF dB, and conversion gain dB. The measured VGA range is 60 dB. The measured S11 is reported in Fig. 12.

The wanted and image signal after downconversion performed by the GPS radio are reported in Fig. 13 for one sample Measured over a 4-MHz band for 15 samples, IR is always higher than 30 dB.

The PLL with its on-chip loop filter has been characterized and the total phase noise, integrated between 500 Hz and 1.5 MHz, is below 7 rms in all measured samples (Fig. 14). Another version of the GPS radio has been integrated in a pure CMOS process (i.e., low resistivity substrate and low quality factor on-chip inductors) in order to experimentally verify the technology portability of this solution. No significant changes have been observed.

TABLE II  
RX CHAIN

	Unity	Spec	Meas
Input RF	GHz	1.575	1.575
Voltage Gain	dB	85	81
VGA range	dB	60	60
S11	dB	< -10	< -12
Noise Figure NF	dB	5	5.3
Image Reject. IR	dB	30	30
P1dB (Min Gain)	dBm	-28	-28
LO leak. to RF	dBm	<-60	-66
Power	mW	<20	18.7

TABLE III  
SYNTHESIZER AND LO BUFFERS

	Unity	Spec	Meas
LO Freq	GHz	1.565	1.565
PhaseNoise @1MHz	dBc/Hz	-95	-95
Phase Noise int. [500Hz-1.5MHz]	rms	<7°	<7°
Band of PLL	KHz	< 500	500
Spurious level	dBc	< -20	< -35
Start-up Time @ferr<10-KHz	ms	<1	<1
Power	mW	<20	16.7

An RF carrier downconverted at IF by the GPS radio is reported in Fig. 15. The most significant spurs (located at the comparison frequency and its harmonics) are smaller than 35 dBc. The frequency response of the RX chain is visible in the same plot as it shapes the thermal noise floor.

A simplified version of the GPS receiver chain that uses an external LO signal has been characterized by soldering an unpackaged die into an application board. The *I-Q* LOs needed by the mixer are generated by an on-chip polyphase filter. The unpackaged RX features  $NF=4$  dB and  $G_0=85$ dB.

It has been experimentally verified that the higher NF and reduced gain in the packaged GPS radio is not due to phase noise of the synthesizer. The worse performance has been attributed primarily to the impedances of the on-chip LO buffer, compared with that of the internal polyphase used to feed the mixer in the unpackaged version. This problem can be easily fixed in a following version.

TABLE IV  
STATE-OF-THE-ART GPS RADIOS

<b>Architecture</b>	<b>Tech (<math>\mu m</math>)</b>	<b>NF/sens</b>	<b>Power (mW)</b>	<b>Area mm<sup>2</sup></b>	<b>Ref</b>
Low-IF – 1.092MHz IMRR=18dB Quad LC VCO	0.35	4dB	27	9.5	1
Low IF – ADC Complex BP filter 32dB IMRR LC VCO	0.25	-130dBm	40	9	2
Low IF – 9.45MHz Active RC IF filter 30dB IMRR Ring Oscillator	0.18	5.3dB	35.4	3.6	<b>This</b>

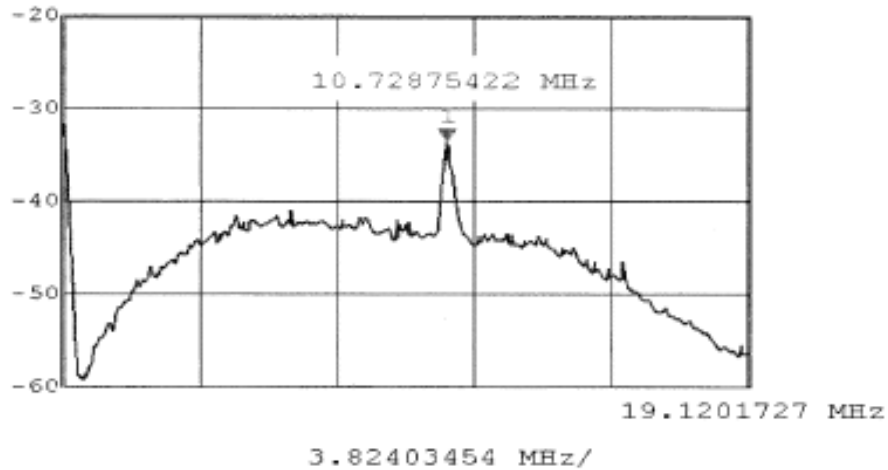


Fig. 16. IF interferer generated by DNS down converted by the GPS radio to IF.

The GPS radio net power consumption is 35.4mW at 1.8 V. A summary of the GPS radio performances is reported in Tables II and III.

The functionality of the GPS radio with DNS generators turned on has also been experimentally verified. The DNS simulates the high-order harmonics produced by the presence on-chip of a baseband processor. The DNS consists of a ring oscillator where it is possible to sweep oscillation frequency and a /4 divider connected to an n + /p substrate diode. Each DNS generator takes 0.34 mm<sup>2</sup>. It has been verified that the chip is always functional and the effect of DNS is negligible.

For frequencies close to the GPS L1 signal, either the  $F_{\text{noise}}$  signal injected by the DNS over supply and ground, or the fourth harmonic of the DNS signal /4 (injected into the substrate diode) is downconverted by the LNA-mixer and amplified by the IF filter (since it falls into the IF band). The

measured amplitude (as shown in Fig. 16) is 33 dBm, therefore, the input signal is 124 dBm.

## 6. CONCLUSION

A comparison with recently published data is reported in Table IV. This GPS radio features the smallest area and the highest level of integration ever reported. The better power performance achieved by [1] can be attributed to the lower IF frequency that allows for a gain-bandwidth reduction in the IF filters opamps and the use of a low-power (but large area) quadrature *LC* VCO instead of a ring oscillator. As pointed out, the small die area and the high level of integration of this GPS radio are due to design and architectural choices (single-ended LNA, ring oscillator VCO with internal loop filter, and active *RC* filter) and, to a smaller extent, to the 0.18- $\mu$  m process used. The chosen approach resulted a net power consumption of 35.4 mW.

The feasibility of a fully integrated 3.6-mm<sup>2</sup> CMOS GPS radio with RF performance suitable for active antenna applications has been reported. The next step is the single-chip integration of the GPS radio together with a digital baseband processor.

## 7. REFERENCES

- [1] F. Behbahani *et al.*, “A 27-mW GPS Radio in 0.35- $\mu\text{m}$  CMOS,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 398–399.
- [2] P. Vancorenland *et al.*, “A fully integrated GPS receiver front-end with 40-mW power consumption,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 396–397.
- [3] P. Andreani and H. Sjolund, “Noise optimization of an inductively degenerated CMOS low noise amplifier,” *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 835–841, Sept. 2001.
- [4] J. Crols *et al.*, “An analog integrated polyphase filter for a high performance low-IF receiver,” in *Proc. VLSI Circuits Symp.*, 1995, pp. 87–88.
- [5] C.-H. Park and B. Kim, “A low-noise, 900-MHz VCO in 0.6 $\mu\text{m}$  CMOS,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 586–591, May 1999.

## ABSTRACT

A single-chip CMOS Global Positioning System (GPS) radio has been integrated using only a couple of external passive components for the input matching network and one external reference for the synthesizer. The receiver downconverts the GPS L1 signal at 1575.42 MHz to an IF of 9.45 MHz. The complete front-end and frequency synthesizer section have been integrated: low noise amplifier, image rejection mixer, IF active filter, and the full phase-locked loop synthesizer, including voltage-controlled oscillator and loop filter. The front-end measured performances are 81-dB maximum gain, 5.3-dB noise figure, and >30-dB image rejection. The synthesizer features a phase noise of -95 dBc/Hz at 1-MHz offset and a total integrated phase noise of less than 7° rms in the 500-Hz–1.5-MHz band. The front-end and the synthesizer draw, respectively, 11 and 9 mA from a 1.8-V supply. The architecture of the front-end and synthesizer has been geared to high level of integration and reduction of silicon area at the lowest possible power consumption. Consequently, the one reported here is the smallest and most integrated CMOS GPS receiver reported so far.

## **ACKNOWLEDGEMENT**

I extend my sincere thanks to **Prof. P.V.Abdul Hameed**, Head of the Department for providing me with the guidance and facilities for the Seminar.

I express my sincere gratitude to Seminar coordinator **Mr. Berly C.J**, Staff in charge, for their cooperation and guidance for preparing and presenting this seminar.

I also extend my sincere thanks to all other faculty members of Electronics and Communication Department and my friends for their support and encouragement.

**ANOOP.K.R**

## **CONTENTS**

1)	INTRODUCTION	1
2)	ARCHITECTURE AND SPECIFICATIONS	3
3)	CHIP DESIGN	7
4)	IMPLEMENTATION DETAILS	15
5)	EXPERIMENTAL RESULTS	18
6)	CONCLUSION	22
7)	REFERENCES	23