

## INTRODUCTION

Even though the word DRAM has been quite common among us for many decades, the development in the field of DRAM was very slow. The storage medium reached the present state of semiconductor after a long scientific research. Once the semiconductor storage medium was well accepted by all, plans were put forward to integrate the logic circuits associated with the DRAM along with the DRAM itself. However, technological complexities and economic justification for such a complex integrated circuit are difficult hurdles to overcome. Although scientific breakthroughs are numerous in the commodity DRAM industry, similar techniques are not always appropriate when high-performance logic circuits are included on the same substrate. Hence, eDRAM pioneers have begun to develop numerous integration schemes. Two basic integration philosophies for an eDRAM technology are:

- Incorporating memory circuits in a technology optimized for low-Cost high performance logic.
- Incorporating logic circuits in a technology optimized for high- Density low performance DRAM.

This seemingly subtle semantic difference significantly impacts mask count, system performance, peripheral circuit complexity, and total memory capacity of eDRAM products. Furthermore, corporations With aggressive commodity DRAM technology do not have expertise in the design of complicated digital functions and are not able to assemble a design team to complete the task of a truly merged DRAM-logic product. Conversely, small application specific integrated circuit (ASIC) design corporations, unfamiliar with DRAM- specific elements and design practice, cannot carry out an efficient

merged logic design and therefore mar the beauty of the original intent to integrate. Clearly, the reuse of process technology is an enabling lhetor en route to cost-effective eDRAM technology. By the same. account, modern circuit designers should be familiar with the new elements of eDRAM technology so that they can efficiently reuse DRAM-specific structures and elements in other digital functions. The reuse of additional electrical elements is a methodology that will make eDRAM more than just a memory' interconnected to a few million Boolean gates.

In the following sections of this report the DRAM applications and architectures that are expected to form the basis of eDRAM products are reviewed. Then a description of elements found in generic eDRAM technologies is presented so that non-memory-designers can become familiar with eDRAM specific elements and technology. Various technologies used in eDRAM are discussed. An example of eDRAM is also discussed towards the end of the report.

It can be clearly seen from this report that embedded DRAM macro extends the on-chip capacity to more than 40 MB, allowing historically off-chip memory to be integrated on chip and enabling System-on-a-Chip (SoC) designs. 'By these memory integrated, on chips, the bandwidth is increased to a high , extend. A highly integrated DRAM approach also simplifies board design, hereby reducing overall system cost and time to market. Even, more importantly, embedding DRAM enables higher bandwidth by allowing a wider on-Chip buss and saves power by eliminating DRAM I/O.

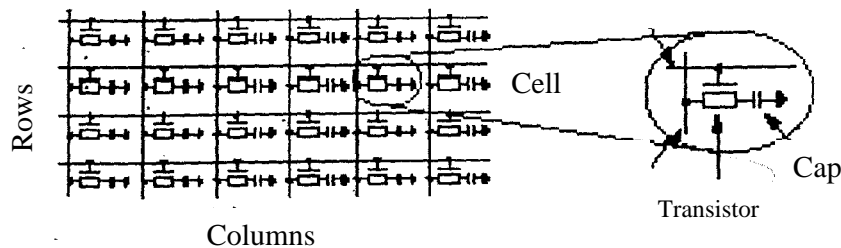
## **WHY embedded DRAM?**

As application-specific integrated circuit (ASIC) technologies expand into new markets, the need for denser embedded memory grows. To accommodate this increase demand, embedded DRAM macros have been offered in state-of-the-art ASIC library portfolios. It can be made clear from this report that embedded DRAM macro extends the on-chip capacity largely, allowing historically off-chip memory to be integrated on chip and enabling System-on-a-Chip (SoC) designs. With memory on the chip, applications can take advantage of the high bandwidth naturally offered by a wide-I/O DRAM and achieve data rates greater than those previously limited by pin count and off-chip pin rates. Applications for this memory include network processors, digital signal processors, and cache chips for microprocessors. The integration of embedded DRAM into ASIC designs intensified the focus on how best to architect, design, and test a high-performance, high density macro as complex as dynamic RAM in an ASIC logic environment. The ASIC environment itself presents many difficult elements that have historically challenged DRAMs—specifically wide voltage axial temperature operating ranges and uncertainties in surrounding noise conditions. These challenges dictate a robust architecture that is noise-tolerant and can operate at high voltage for performance and at low voltage for reduced power. With the advent of embedded DRAM offerings in a logic-based ASIC technology, the performance of embedded DRAM macros has improved significantly over that of DRAM-based technologies

### **Fundamental DRAM operation**

Embedded DRAM working can be explained effectively starting with DRAM working. DRAM memory arrays are composed of wordlines (or rows) and bitlines (columns); At the crosspoint of every row and column is a storage cell consisting of a transistor and capacitor. The data state of the cell is stored as charge on the capacitor, with the transistor acting as a switch controlling access

to the capacitor. With the switch on (wordline activated), charge can be read from or written to the storage cell. The rest of the DRAM support circuits are dedicated to controlling the wordlines and bitlines to -read and write the memory array.



## Embedded DRAM Technologies

The three commonly identified types of embedded DRAM are DRAM based, blended (or hybrid), and logic-based. DRAM-based I is practically the same as commodity DRAM—using DRAM periphery devices to build logic circuitry with perhaps the addition of one or two metal layers for logic routing. Blended technology uses additional front-end masks to enhance the performance of the DRAM periphery devices, to speed up logic performance. Logic-based embedded DRAM enables transistors with performance compatible with leading-edge logic processes, resulting in an improved DRAM logic interface, and an on-chip logic performance path to implementing system on-chip designs.

System designers are turning to embedded DRAM for several reasons. Unlike commodity DRAMs, which are only available in a standard range of densities—typically 4, 16 and 64 Mbits—the exact amount of memory required in a system can be specified in .the embedded DRAM macro block, for example, 5, 9, or 17 Mbits. Thus, no memory is wasted and area and cost are opt In

addition, the exact configuration and memory interfaces can be specified in the macrocell, thus offering flexibility and optimum system performance.

Each of these three types combines the functions of both memory and logic on a single die. The elimination of the additional I/O bonding pads required for two separate chips saves about 5 to 10 percent of overall silicon area over discrete solutions. It can also help relieve the pad limitation problem of complex ICs by providing pad savings over discrete ICs, since DRAM driving pads are eliminated from both memory and logic parts. Depending on the particular design, an embedded array requires far fewer pads, thus saving space. This space saving is even more significant for smaller designs of 300K logic gates and below, because it alleviates the pad limitation problem common in these designs.

### **DRAM-based Embedded DRAM**

DRAM-based embedded DRAM chips begin with DRAM process architecture, usually one with two metal layers, on top of which one extra metal layer is added for logic routing. The philosophy behind this type of embedded DRAM is usually the same as that employed by discrete commodity DRAM manufacturers. This is to make the cell as small as possible, since a smaller cell means a smaller die, and thus a less expensive one.

Typically, the DRAM cell size is 50 to 100 percent smaller than a cell of logic-based technology of the same generation. However, in this approach the peripheral circuitry used for logic design is the same as commodity-based DRAM circuitry. The high thermal cycles introduced in the DRAM-based process, just before the first metal level is processed, induce the diffusion of transistor dopants. This induced diffusion degrades device performance.

The use in commodity DRAM of polycide in the polysilicon gate makes it impossible to introduce an advanced PMOS device. Polycide is necessary in order to make a self-aligned bitline contact in the DRAM cell, thus eliminating otherwise necessary design rule space between the transfer gate and the bitline contact, and reducing the cell size by at least 20 percent. In fact, because of this self-aligned contact, commodity DRAM can use only buried-channel PMOS, a technology that became extinct in logic processes after the 0.35-micron generation.

For these reasons, performance-wise, DRAM-based technology lags logic technology by at least two generations. For example, the performance of devices from 0.18-micron DRAM-based transistors is roughly equivalent to the performance of cutting-edge 0.35-micron logic process

### **Blended Embedded DRAM**

Blended, or hybrid, embedded DRAM is very similar to the DRAM-based type, but it is constructed with a couple of additional mask layers to enhance the DRAM periphery devices, which also serve as logic transistors. In essence, a blended process incorporates some additional steps lacking in a commodity DRAM process, in order to enhance the performance of peripheral circuitry. Normally, this involves slightly reducing the after transistor thermal cycle and thereby reducing dopant diffusion; adding a source/drain suicide process outside of the DRAM array; and more aggressively reducing the channel lengths of peripheral transistors. But the blended embedded DRAM process architecture still looks much more like a DRAM-based device than a logic-based device because of features such as buried channel PMOS transistors, and possibly polycide instead of silicide gates.

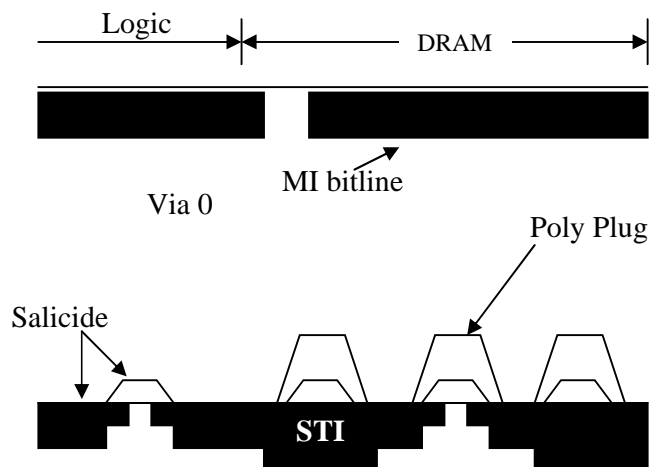
Yet hybrid, like the DRAM-based process, is not library-compatible with logic. Therefore, designs with logic processes can't easily be ported to DRAM-based and hybrid processes, without re-designing the logic circuits. This is because system designers usually design a standalone logic chip first, and only later make the decision to create a second, embedded logic design for a more optimized, or higher-end, product offering.

The hybrid device speed/power figure of merit is closer to 1.5 generations behind that of logic than the two generations behind of DRAM based embedded DRAM. For example, the performance of 0.18-micron DRAM based technology is roughly equivalent to 0.35-micron logic and 0.22-micron - hybrid embedded DRAM. Note, however, that when comparing figures of merit, that several variables are involved, such as speed, power dissipation, design rule, and gate density. There are a wide range of hybrid types that have been introduced by manufacturers worldwide and their performances vary depending on the approach.

### **Logic-Based Embedded DRAM**

Logic-based embedded DRAM derives from an existing logic process, so it has exactly the same design rules and SPICE models as the advanced standalone logic technology. Thus, there is no sacrifice of speed, as the speed/power figure of merit is exactly the same as the derivative logic process. Logic library compatibility also allows any design tested in a standalone logic technology to be easily ported into a logic-based embedded DRAM implementation without modification. In addition, logic-based embedded DRAM utilizes extensive libraries developed for standalone logic, thus making logic-based DRAM designs more convenient for designers.

Knowing which approach is best is usually a simple task. For example, if the chip layout is dominated by logic, logic-based designs are more economical because logic design rules are denser than those of commodity DRAM periphery device. But if the area balance shifts, towards the DRAM array; DRAM-based or hybrid designs are more – economical, even though they cannot offer performance as good as logic-based embedded DRAM designs.



It is possible to produce a small DRAM cell in a 0.18-micron logic-based embedded DRAM process. The approach shown in Figure utilizes a self-aligned polysilicon bitline contact and polycided- wordline. This allows a higher performance DRAM array, as well as a smaller cell. Yet, the -DRAM structure utilizes metal as a bitline. This approach is good for reducing mask count and wafer cost. In fact, it allows the removal of at least two critical masks, compared to a commodity DRAM front-end process. Moreover, the resistance of a metal bitline is lower than that of a conventional polycide bitline typically used in -commodity DRAM, - thereby allowing higher speed and lower power dissipation. Finally, the logic circuitry is similar to conventional logic technology, utilizing cobalt salicide, dual-gate poly (p + poly NMOS and n + poly PMOS), and abrupt p-n junctions for high performance.

## ARCHITECTURE

The commodity DRAM industry has clearly led the way in the advancement of silicon process technology. In addition, many circuit architectures evolved as a direct result of the DRAM technology progression. Examples of PRAM specific architectures, which are expected to form the basis of the first eDRAM circuits, are as follows Three categories of DRAM architectures discussed are:

- Asynchronous
- Synchronous
- Interface-related

Asynchronous DRAM design techniques are commonly referred to as Fast Page (FP) mode and extended data output (EDO) mode. These two architectures were the first developed for the DRAM industry. They both rely on input signals known as the column address strobe (CAS) and row address strobe (RAS) to move address signals into and out of the DRAM memory cell array These types of memories produce an image of the stored data at a fixed time after the strobe edges of RAS and CAS. Both circuits have the ability to randomly access any single digit of binary data, as well as to sequentially access particular columns of data resident on a currently accessed row address.

Synchronous design is a second-generation approach intended to enhance the temporal interface between DRAM and microprocessor. Synchronous DRAM (SDRAM) or double-data rate synchronous DRAM (DDR SDRAM) require the use of a master clock in addition to the CAS and RAS strobes. In these memories, the flow of address and data signals through the different sub- circuits within the memory are carefully controlled by the rising and falling edges of the master clock. Although asynchronous design does not necessarily reduce the access time to 'the first bit of random data, it does enhance the throughput of subsequent data because of:

- Efficiency in latching input signals
- Reduced complexity of internally generated timing edges
- The ability to use sequentially activated memory arrays

Interface- related designs are protocol intensive designs that have been developed to enhance synchronous communications between integrated circuits. These types of architectures may dominate the commodity DRAM industry, and they are referred to by names like Rambus, Ramlink, and Synlink. Once DRAM and logic reside on a monolith, there will be less of a need for high-performance interchip protocols because bandwidth limitations will be alleviated due to wider Internal bus However, as simple eDRAM circuits become complicated systems on a chip (SOC), and because direct memory access will be an essential testing requirement, protocols like these will continue to be useful.

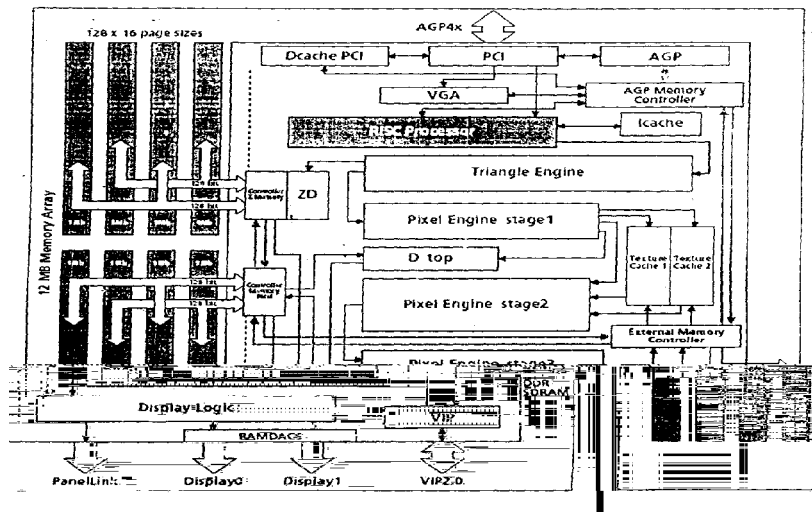
### **An Example of eDRAM**

Micron's - San Jose Design Center recently demonstrated working silicon for a new class of semiconductor components, those integrating high— density commodity DRAM blocks with complex standard. cell based logic into a single chip. Embedding DRAM cores into logic chips paves the way for the next wave of chips, providing higher performance solutions for networking and computing markets via higher memory band widths / clock speeds and lower power/ miniaturization for consumer and- communication markets. This first embedded DRAM chip developed by Micron is a 3D/2D graphics and video accelerator originally targeted at the PC graphics market. The project primarily proved that scientists could embed highly complex logic, SRAM, and thus leading industry of DRAM technology into a single integrated monolithic device. Further, basing this embedded technology on low- cost commodity DRAM process permitted to

achieve dramatic cost and performance benefits over other approaches. Micron built the chip with a System-on-a-Chip (SOC) design approach and architecture, simplifying the design effort and establishing a platform for faster development of follow-on eDRAM chips. They composed the basic eDRAM SOC architecture as a collection of logic and DRAM memory blocks around a highbandwidth ring bus, an architecture that enables high-speed design of large chips with multiple clock domains across significant die with the use of buffered clocks and signals. The SOC design approach also focuses on the integration of IP blocks from a variety of internal Micron and external vendors. For example, Micron's UKDC delivered a RISC processor and PLL and Micron's DRAM group delivered the RAMCore as hard cores, whereas external vendors delivered the: VGA, AGP, and PCI blocks as soft cores. The V4400e chip's design and architecture is a fine example of embedded DRAM technology and integrated silicon.

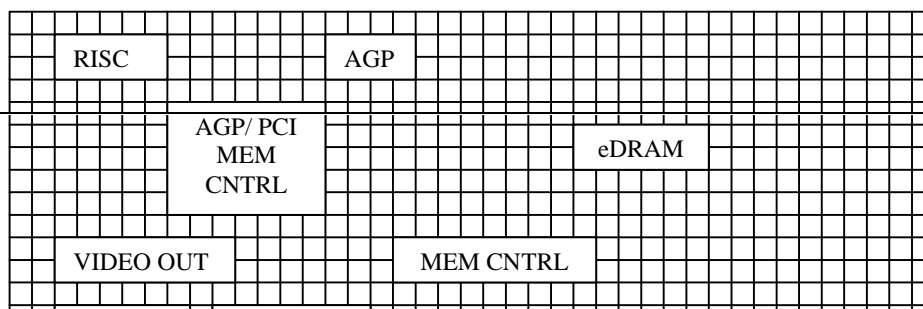
### **V4400e Chip**

Within a 480-pin BGA package, the V4400e chip contains an impressive 127 million transistors, with nearly a third of the die devoted to DRAM. Note that the number of transistors exceeds many of the most popular large microprocessors of today, such as Intel's 43 million transistor P4. The V4400e has 3.5 million equivalent NAND logic gates and 12MB of DRAM constructed as an array of twelve 1MB RAMCore blocks. Each DRAM megabyte block is 5mm by 1.4mm, or 7mm<sup>2</sup>, in 0.18Dm technology. Now designs with 0.15Dm DRAM blocks, achieving 4mm<sup>2</sup> are also available. Memory red techniques are used to maintain high yield. The prototype was fabricated in 0.25 logic and 0.18Em memory, yielding the die size of 18.4 x 18.4mm<sup>2</sup>, which would be less than 10 x 10mm<sup>2</sup> in today's embedded DRAM technology.



V4400e Embedded DRAM Graphics Controller chip Architecture and Block Diagram

The goal of the V4400e project from the silicon technology viewpoint was to prove that there was a path to integrate our highly efficient DRAM design and production capability with logic designs typical of today's ASIC efforts. And, further, once a process for that integration was established, to identify 'and address the inefficiencies in the design process and methodologies to become the pre-eminent provider of integrated memory and logic Intellectual Property (IP). The goal of the V4400e project from the graphics semiconductor viewpoint was to produce an industry competitive graphics chip. The features and performance of PC graphics accelerators has increased dramatically over the last seven years. Therefore, a competitive offering must render complex scenes with peak rendering rates approaching a Gig pixel per second and sustained rendering rates for common operations of hundreds of million<sup>3</sup>. pixels per second. Thus a full-featured chip with the ability to sustain 400 Mega pixels per second is almost achieved.



Since most common rendering operations require reading and/or writing around seven to ten 32-bit words per pixel, Micron designed a part with 16GB of aggregate memory bandwidth, courtesy of a large array of embedded DRAM, to meet the goal. At the start of this design no previous graphics chip had employed embedded DRAM. Even with 256-bit busses, requiring nearly 400 pins, and 200 MHz DDR SDRAM can achieve only around 6 GB/s of aggregate memory bandwidth, which seriously limits their sustained rendering rates. With these extreme memory bandwidth requirements satisfied, by embedded DRAM and the attendant package and silicon savings, the technical advantages of embedded DRAM in the graphics market seemed apparent.

### **Specific Advantages of the V4400e eDRAM**

Embedded DRAM can offer many advantages over use of external DRAM components in the design of electronic systems. These advantages include:

1. Lower power and higher frequency signals between the logic and the DRAM since

- (a) The external drive circuitry in both the DRAM and the ASIC chips are eliminated
- (b) More effective control of the DRAM/banks can result when additional signaling is used between the DI and processing logic

2. Miniaturization and cost reduction of the solution by elimination of chips and use of the specific amount of memory called for by the application, which becomes increasingly wasteful in both cost and power as commodity DRAMs increase in size

3. Significantly improved transfer bandwidth between the memory and processing logic due to use of exceptionally wide buses (literally thousands of signals)- not possible when constrained by conventional packaging limitations of a few hundred pins.

## **APPLICATIONS AND BENEFITS**

Generally speaking, embedded DRAM is especially applicable to system-on-chip (SoC) designs because it integrates memory and logic on a single die; reduces total chip count in a system; reduces power consumption; and increases performance. DRAM—based and blended embedded DRAM technologies are often used in applications that require high—density memory in a small area. Typically, these are systems with up to 128 Mbits of memory in a 0.18-micron process technology. These two technologies are also best for applications that are more cost-sensitive. A system design that requires considerably more memory than supporting on-chip logic, is an ideal candidate for DRAM-based or hybrid technology, especially from a cost standpoint. Such applications include CD-ROM, DVD-ROM, disk drives, printers, lower-end graphics, IO/100-Mbits/sec switches, replacements for standalone SRAM, and custom-designed DRAMs. A

major benefit of logic-based embedded DRAM is higher performance. Thus, logic-based technology is often used in high-performance applications such as high-end consumer and networking. Applications that depend on video signal encoding, such as digital video cameras, laptop PC graphics, smart cellular phones and PDAs, also benefit from logic-based embedded DRAM. Lower power dissipation, another major embedded DRAM benefit, further advocates using this technology for portable applications. In addition, some very fast custom memory designs are now possible using this technology. Because commodity memory standards do not apply to embedded DRAM, embedded DRAM is more flexible to use. Specialized designs can thus be created that are oriented toward speed, bandwidth and low power, rather than the emphasis on low price and efficiency that have historically been the aims of the DRAM macrocell. Architectural innovations made possible by this technology include bandwidth DRAM with a very wide bus for handling a lot of parallel data, which is used in high-end graphics applications and networking switches. Other designs emulate SRAMs with fast random rather than the typical DRAM page—mode access.

As the task of merging DRAM and logic would suggest, several partnerships (e.g., Toshiba-IBM-Infineon and Mitsubishi-NeoMagic) merged their resources in technology and design for the experiments with applications involving CDRAM. These corporations appreciate the numerous reasons for using eDRAM. Specific examples in support of the desire to include the DRAM storage medium on the same integrated circuit as the control execution units of classic computer architectures are:

- Form factor: reduces the number of chips per board and total Volume consumed

- Performance: avoids interchip propagation delays and interchip bandwidth bottlenecks
- Power: avoids interchip Interface power consumption and narrow high-speed buses
- Parallelism: increases the number of bits per logic bus
- Modularity: freedom to choose an optimal size memory for a particular application
- Availability: never being left out of the commodity DRAM technology progression
- Parity: avoiding the use of parity bits for the purpose of interchip communications

In mid-1997, the first eDRAM products involved digital signal proc for graphics applications. The graphics industry is expected to continue as a leader in the use of eDRAM because of a natural migration from a two dimensional to a three algorithm, and the need to enhance display resolution. In these products, total memory capacity and speed of data access are expected to require 64 Mb memories and bus widths of 256 parallel conductors.

Network applications like routers and asynchronous transfer mode (ATM) switches will require very complex and high-performance logic functions in addition to the memory capacity and bus sizes required by the graphics applications. The hard disk drive (HDD) market requires a less ambitious demand on total memory capacity per integrated circuit, but a highly cost-competitive spirit will accompany their eDRAM requirements. Once the cost of eDRAM technology becomes reasonable, designers of numerous applications such as printers fax machines, camcorders, and handheld games are expected to desire eDRAM technology simply because their systems can be designed with fewer components. The above-mentioned applications all have an intrinsic need

for large amounts of memory and at least one other good reason to embed memory. The use of eDRAM in these particular applications will only be gated by cost structures that are preexisting. Emerging applications like wireless communicators represent new products that are more open to the use of new memory technology. The advent of the Wireless Application Protocol (WAP), presently defined - and used in Nokia and Ericsson communicators, will provide Internet browsing services requiring memory on the order of 64 Mb with low power dissipation and a small form factor. In this type of product, there are more than three reasons to justify eDRAM technology.

## CONCLUSION

After more than 30 years of process development, the DRAM storage medium can now be integrated on the same substrate containing meaningful amounts of high- performance Boolean logic. Embedded DRAM technology offerings will support memory sizes up to 64 Mb with little constraint associated with its minimum size or modularity and high-performance logic functions (over a million Boolean gates). Applications Using such eDRAM technology can expect an increase of a factor of 3 in data bandwidth, owing to the increased number of parallel bus bits. Trade-offs between bandwidth and power dissipation are expected to dramatically favor v products that use eDRAM. System designers need to be aware that cost structures and performance trade-offs of eDRAM solutions are varied. However, judicious reuse of eDRAM structures and elements in the non-memory portion of an integrated circuit is a way to amortize additional technology cost. In support of this strategy:

- The isolated P-TUB can be used as an effective shield of electrical noise that flows below the silicon surface.
- The self-aligned contact reduces the separation between the source drain contact and the gate; when used in conjunction with the tungsten local interconnect a dramatic increase in packing density will result.
- The redundancy scheme can be used as a trimming element in circuits that require accurate tolerances.
- The low-leakage access transistor can be used in the design of low power electronics provided high performance is not required
- The 3D capacitor of eDRAM technology can be an effective analog capacitor provided its range of operation is limited to the voltage specified by the particular oxide thickness of the eDRAM technology being used.

Traditionally, in cost-sensitive consumer applications, large memory arrays of 64 megabits and above were usually better suited to discrete commodity memory implementations. But as the supply of low-density DRAM wanes and prices rise, system designers are finding that embedding DRAM densities of 16 Mbytes and below is more cost effective per chip than discrete alternatives

In summary, embedded DRAM is becoming more common in consumer and communications applications because of its superior performance, silicon area and low power compared to discrete memory solutions. Embedding DRAM -enables higher bandwidth by a wider on-chip bus. Therefore, an increasing number system are using it particularly for high performance or low-Power applications requiring memory buffers with fast access, such as networking, high-end digital con and portable applications. As with other approaches, test issues still exist, combined test approach based on the requirements design can improve cost and throughput. Since companies have successfully implemented eDram in many of their commodities

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## **ABSTRACT**

Dynamic random access memory (DRAM) has been offered as a commodity product by dozens of companies for more than 30 years in no less than seven different generations of MOSFET technology. Presently, DRAM products appear in almost every electronic function that is governed by the theory of Boolean logic. Plans to integrate the DRAM storage medium with various digital functions have been contemplated for a long time. These attempts have been successful to a large extent. Many companies have already entered in to this field of embedded technology. With memory on the chip, applications can take advantage of the high bandwidth naturally offered by a wide-I/O DRAM and achieve data rates greater than those previously limited by pin count and off-chip pin rates. The constructional features, advantages, disadvantages, applications etc are reviewed in this report. The use of embedded DRAM technology has become widespread, especially in higher-end system designs, because of its superior performance, silicon area savings, and low power compared to discrete memory solutions.

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